EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	989	703/14.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 16:41
L2	402	(model adj check$3) and @ad<"20010113"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 17:14
L3	50	L2 and trace	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 17:17
L4	20	L2 and disjoint	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 17:18
L5	3	(disjoint adj trace$1) and @ad<"20010113"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 17:21
L6	421	(multiple adj trace$1) and @ad<"20010113"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 17:21

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(mutually-disjoint or (mutually adj disjoint) and trace$1 and model).clm.	US-PGPUB	OR	OFF	2006/05/20 18:03
L2	1	(mutually-disjoint or (mutually adj disjoint) and trace$1).clm.	US-PGPUB	OR	OFF	2006/05/20 18:03
L3	5	(mutually-disjoint or (mutually adj disjoint)).clm.	US-PGPUB	OR	OFF	2006/05/20 18:03
L4	3	((reachable adj set$1) and trace$1 and intersection$1).clm.	US-PGPUB	OR	OFF	2006/05/20 18:08
L5	3	(disjoint and intersection$1 and trace$1 and intersection$1).clm.	US-PGPUB	OR	OFF	2006/05/20 18:08

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6691078".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 18:11
L2	136	(disjoint near path$1) and @ad<"20010113"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/05/20 18:12

Results for "((model check*<and>multiple trace*)) <and> (pyr >= 1951 <and> pyr <= 2001)"
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Modify Search

((model check*<and>multiple trace*)) <and> (pyr >= 1951 <and> pyr <= 2001) Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **Static analysis and dynamic steering of time-dependent systems**
Vicario, E.;
Software Engineering, IEEE Transactions on
Volume 27, Issue 8, Aug. 2001 Page(s):728 - 748
Digital Object Identifier 10.1109/32.940727
AbstractPlus | References | Full Text: PDF(1496 KB) IEEE JNL
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Results for "((model check*<and>disjoint trace*)) <and> (pyr >= 1951 <and> pyr <= 2001)"
Your search matched 0 documents.
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Modify Search

((model check*<and>disjoint trace*)) <and> (pyr >= 1951 <and> pyr <= 2001) Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

No results were found.

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Results for "((model check*<and>trace*)<and>disjoint) <and> (pyr >= 1951 <and> pyr <..."
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Modify Search

((model check*<and>trace*)<and>disjoint) <and> (pyr >= 1951 <and> pyr <= 2001) Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1-25 | 26-43

1. **Handling obstacles in goal-oriented requirements engineering**
van Lamsweerde, A.; Letier, E.;
Software Engineering, IEEE Transactions on
Volume 26, Issue 10, Oct. 2000 Page(s):978 - 1005
Digital Object Identifier 10.1109/32.879820
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Burch, J.R.; Clarke, E.M.; Long, D.E.; McMillan, K.L.; Dill, D.L.;
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4. **A logical characterization of bisimulation for labeled Markov processes**
Desharnais, J.; Edalat, A.; Panangaden, P.;
Logic in Computer Science, 1998. Proceedings. Thirteenth Annual IEEE Symposium on
21-24 June 1998 Page(s):478 - 487
Digital Object Identifier 10.1109/LICS.1998.705681
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Fabrega, F.J.T.; Herzog, J.C.; Guttman, J.D.;
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15. **Reliable software and communication. I. An overview**
Chung, F.R.K.;
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Tahar, S.; Xiaoyu Song; Cerny, E.; Zijian Zhou; Langevin, M.; Ait-Mohamed, O.;
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Girault, A.; Bilung Lee; Lee, E.A.;
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Relevance scale

1 A practical method for verifying event-driven software

Gerard J. Holzmann, Margaret H. Smith

May 1999 **Proceedings of the 21st international conference on Software engineering**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.40 MB) Additional Information: full citation, references, citings, index terms

Keywords: case studies, feature interactive, formal methods, model checking, reactive systems, software testing, software verification, telephone call processing

2 Using model checking to generate tests from requirements specifications

Angelo Gargantini, Constance Heitmeyer

October 1999 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 7th European software engineering conference held jointly with the 7th ACM SIGSOFT international symposium on Foundations of software engineering ESEC/FSE-7**, Volume 24 Issue 6

Publisher: Springer-Verlag, ACM Press

Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, citings, index terms

Recently, many formal methods, such as the SCR (Software Cost Reduction) requirements method, have been proposed for improving the quality of software specifications. Although improved specifications are valuable, the ultimate objective of software development is to produce software that satisfies its requirements. To evaluate the correctness of a software implementation, one can apply black-box testing to determine whether the implementation, given a sequence of system inputs, produces the ...

3 Bandera: extracting finite-state models from Java source code

James C. Corbett, Matthew B. Dwyer, John Hatcliff, Shawn Laubach, Corina S. Păsăreanu, Robby, Hongjun Zheng

June 2000 **Proceedings of the 22nd international conference on Software engineering**

Publisher: ACM Press

Full text available: pdf(345.15 KB) Additional Information: full citation, abstract, references, citings, index terms

Finite-state verification techniques, such as model checking, have shown promise as a cost-effective means for finding defects in hardware designs. To date, the application of these techniques to software has been hindered by several obstacles. Chief among these is the problem of constructing a finite-state model that approximates the executable behavior of the software system of interest. Current best-practice involves hand-construction of models which is expensive (prohibitive for all but ...

Keywords: abstract interpretation, model checking, model extraction, program specialization, program verification, slicing

4 Three approximation techniques for ASTRAL symbolic model checking of infinite state real-time systems

Zhe Dang, Richard A. Kemmerer

June 2000 **Proceedings of the 22nd international conference on Software engineering**

Publisher: ACM Press

Full text available: pdf(359.05 KB) Additional Information: full citation, abstract, references, citings, index terms

ASTRAL is a high-level formal specification language for real-time systems. It has structuring mechanisms that allow one to build modularized specifications of complex real-time systems with layering. Based upon the ASTRAL symbolic model checler reported in [13], three approximation techniques to speed-up the model checking process for use in debugging a specification are presented. The techniques are random walk, partial image and dynamic environment generation. Ten mutation tests on a rai ...

Keywords: ASTRAL, formal methods, formal specification and verification, model checking, real-time systems, state machines, timing requirements

5 HSIS: a BDD-based environment for formal verification

A. Aziz, F. Balarin, S.-T. Cheng, R. Hojati, T. Kam, S. C. Krishnan, R. K. Ranjan, T. R. Shiple, V. Singhal, S. Tasiran, H.-Y. Wang, R. K. Brayton, A. L. Sangiovanni-Vincentelli

June 1994 **Proceedings of the 31st annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(91.11 KB) Additional Information: full citation, references, citings, index terms

6 Verification of time partitioning in the DEOS scheduler kernel

John Penix, Willem Visser, Eric Engstrom, Aaron Larson, Nicholas Weininger

June 2000 **Proceedings of the 22nd international conference on Software engineering**

Publisher: ACM Press

Full text available: pdf(111.58 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes an experiment to use the Spin model checking system to support automated verification of time partitioning in the Honeywell DEOS real-time scheduling kernel. The goal of the experiment was to investigate whether model checking could be used to find a subtle implementation error that was originally discovered and fixed during the standard formal review process. To conduct the experiment, a core slice of the DEOS scheduling kernel was first translated without abstraction ...

7 Decoupling synchronization from local control for efficient symbolic model checking of statecharts

William Chan, Richard J. Anderson, Paul Beame, David H. Jones, David Notkin, William E. Warner

May 1999 **Proceedings of the 21st international conference on Software engineering**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.31 MB) Additional Information: full citation, references, citings, index terms

Keywords: binary decision diagrams, fault tolerance, formal methods, formal verification, software specification, statecharts, symbolic model checking

8 Fault origin adjudication

Karthikeyan Bhargavan, Carl A. Gunter, Davor Obradovic

August 2000 **Proceedings of the third workshop on Formal methods in software practice**

Publisher: ACM Press

Full text available: pdf(522.20 KB) Additional Information: full citation, abstract, references, citings, index terms

When a program P fails to satisfy a requirement R supposedly ensured by a detailed specification S that was used to implement P, there is a question about whether the problem arises in S or in P. We call this determination fault origin adjudication and illustrate its significance in various software engineering contexts. The primary contribution of this paper is a fra ...

9 Formal verification of FIRE: a case study

Jae-Young Jang, Shaz Qadeer, Matt Kaufmann, Carl Pixley

June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**

Publisher: ACM Press

Full text available: pdf(93.19 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We present our experiences with the formal verification of an automotivechip used to control the safety features in a car. We useda BDD based model checker in our work. We describe our verificationmethodology for verifying a very complicated property on arelatively large design. We also describe the bugs that were foundand present our views on how to make model checking an effectiveintegrated part of the design flow for complex hardware systems.

10 Using the ASTRAL model checker to analyze mobile IP

Zhe Dang, Richard A. Kemmerer

May 1999 **Proceedings of the 21st international conference on Software engineering**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.16 MB) Additional Information: full citation, references, citings, index terms

Keywords: ASTRAL, Encryption protocols, formal methods, formal specification and verification, real-time systems, state machines, timing requirements

11 Forward model checking techniques oriented to buggy designs

Hiroaki Iwashita, Tsuneo Nakata

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(91.22 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Forward model checking is an efficient symbolic model checking method for verifying realistic properties of sequential circuits and protocols. In this paper, we present the techniques that modify the order of state traversal on forward model checking, and that dramatically improve average CPU time for finding design errors. A failing property has to be checked again and again to analyze the bug until it is corrected. The techniques, therefore, can have significant impacts on actual verification ...

Keywords: formal verification, symbolic state traversal, symbolic model checking, forward model checking

12 Alcoa: the alloy constraint analyzer

Daniel Jackson, Ian Schechter, Hya Shlyahter

June 2000 **Proceedings of the 22nd international conference on Software**

engineering
Publisher: ACM Press

Full text available: pdf(145.10 KB) Additional Information: full citation, abstract, references, citings, index terms

Alcoa is a tool for analyzing object models. It has a range of uses. At one end, it can act as a support tool for object model diagrams, checking for consistency of multiplicities and generating sample snapshots. At the other end, it embodies a lightweight formal method in which subtle properties of behaviour can be investigated.Alcoa's input language, Alloy, is a new notation based on Z. Its development was motivated by the need for a notation that is more closely tailored to ob ...

Keywords: constraint satisfaction, formal specifications, model checking, object models, relational logic, software analysis

13 Fitting formal methods into the design cycle

K. L. McMillan
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(325.61 KB) Additional Information: full citation, references, citings, index terms

14 A formal basis for architectural connection

Robert Allen, David Garlan
July 1997 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 6 Issue 3
Publisher: ACM Press

Full text available: pdf(463.23 KB) Additional Information: full citation, abstract, references, citings, index terms, review

As software systems become more complex, the overall system structure—or software architecture—becomes a central design problem. An important step toward an engineering discipline of software is a formal basis for describing and analyzing these designs. In the article we present a formal approach to one aspect of architectural design: the interactions among components. The key idea is to define architectural connectors as explicit semantic entities. These are specified as a col ...

Keywords: WRIGHT, formal models, model-checking, module interconnection, software analysis

15 Speeding up symbolic model checking by accelerating dynamic variable reordering

Christoph Meinel, Christian Stangier
March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**
Publisher: ACM Press

Full text available: pdf(500.80 KB) Additional Information: full citation, abstract, references, citings, index terms

Symbolic Model checking is a widely used technique in sequential verification. As the size of the OBDDs and also the computation time depends on the order of the input variables, the verification may only succeed if a well suited variable order is chosen. Since the characteristics of the represented functions are changing, the variable order has to be adapted dynamically. Unfortunately, dynamic reordering strategies are often very time consuming and sometimes do not provide any improvement of ...

16 Safety critical systems based on formal models

Lars Asplund, Kristina Lundqvist
December 2000 **ACM SIGAda Ada Letters**, Volume XX Issue 4
Publisher: ACM Press
Full text available: pdf(732.05 KB) Additional Information: full citation, abstract, index terms

The Ravenscar profile for high integrity systems using Ada 95 is well defined in all real-

time aspects. The complexity of the run-time system has been reduced to allow full utilization of formal methods for applications using the Ravenscar profile. In the Mana project a tool set is being developed including a formal model of a Ravenscar compliant run-time system, a gnat compatible run-time system, and an ASIS based tool to allow for the verification of a system including both COTS and code that ...

17 Verification techniques for cache coherence protocols

Fong Pong, Michel Dubois
March 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 1
Publisher: ACM Press

Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, references, citings, index terms

In this article we present a comprehensive survey of various approaches for the verification of cache coherence protocols based on state enumeration, (symbolic model checking, and symbolic state models. Since these techniques search the state space of the protocol exhaustively, the amount of memory required to manipulate that state information and the verification time grow very fast with the number of processors and the complexity of the protocol mechanism ...

Keywords: cache coherence, finite state machine, protocol verification, shared-memory multiprocessors, state representation and expansion

18 Efficient generation of counterexamples and witnesses in symbolic model checking

E. M. Clarke, O. Grumberg, K. L. McMillan, X. Zhao
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(225.22 KB) Additional Information: full citation, references, citings, index terms

19 Strategic directions in real-time and embedded systems

John A. Stankovic
December 1996 **ACM Computing Surveys (CSUR)**, Volume 28 Issue 4
Publisher: ACM Press
Full text available: pdf(209.23 KB) Additional Information: full citation, references, citings, index terms

20 Formal specification and verification of a dataflow processor array

Thomas A. Henzinger, Xiaojun Liu, Shaz Qadeer, Sriram K. Rajamani
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press

Full text available: pdf(98.54 KB) Additional Information: full citation, abstract, references, citings, index terms

We describe the formal specification and verification of the VGI parallel DSP chip [1], which contains 64 compute processors with ~30K gates in each processor. Our effort coincided in time with the "informal" verification stage of the chip. By interacting with the designers, we produced an abstract but executable specification of the design which embodies the programmer's view of the system. Given the size of the design, an automatic check that even one of the 64 processors sati ...

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[PS] Automated software testing using model-checking - group of 3 »
J Callahan, F Schneider, S Easterbrook - Proceedings 1996 SPIN Workshop, 1996 - cis.upenn.edu
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P Godefroid, P Wolper - Logic in Computer Science, 1991. LICS'91., Proceedings of ..., 1991 - ieeexplore.ieee.org
... i (where S, is the set of states of A,) are pairwise **disjoint**. words accepted by AG (all states of AG considered ac- cepting). We define the **trace** behavior of ...
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... Is your **Model Checker** on Time? ... The complexity of implementation verication for (concurrent) programs is studied in, eg, [39,56,63], where both **trace**- and tree ...
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Using a **model checker** to test safety properties - group of 5 »
P Ammann, W Ding, D Xu - International Conference on Engineering of Complex Computer ..., 2001 - doi.ieeecs.org
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